UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/376,654	08/18/1999	ALAN FOLMSBEE	5437-076/P41	6747

25920	7590	06/14/2005

MARTINE PENILLA & GENCARELLA, LLP
710 LAKEWAY DRIVE
SUITE 200
SUNNYVALE, CA 94085

EXAMINER
LANIER, BENJAMIN E

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/376,654	FOLMSBEE, ALAN
	Examiner	**Art Unit**	
	Benjamin E Lanier	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *11 May 2005* .

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1,3,4,13,17 and 18* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1,3,4,13,17,18* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *18 August 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application (PTO-152)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1.   In view of the Appeal Brief filed on 11 May 2005, PROSECUTION IS HEREBY

REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following

two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37

CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a

supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or

other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 112

2.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

3.   Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing

to particularly point out and distinctly claim the subject matter which applicant regards as the

invention.

4.   Claim 4 recites the limitation "the error correction key" in line 3. There is insufficient

antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6.   Claims 1, 3, 4, 13, 17, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by

Chen, U.S. Patent No. 6,044,483. Referring to claims 1, 17, Chen discloses an error correction

system wherein a personal computer (Col. 6, lines 30-49) contains an error detection unit (Figure

1), which meets the limitation of a central processing unit chip, processor circuitry on said chip,

a programmable error correcting circuit on said chip. The system contains several DRAM units

that store check bits that are used during the error correction process (Col. 11, lines 50-52 &

Figure 1), which meets the limitation of RAM on said chip storing error correcting information,

said RAM being in communication with said programmable error correcting circuit. The error

detection unit performs error detection and correction operations on error correction code words

(Col. 5, lines 3-47). If the error correction code word contains an uncorrectable error then the

instruction with the error correction code word can not be executed, however, if the error is

correctable, then the instruction is executed (Figure 7), which meets the limitation of the

programmable error correcting circuit receives said error correcting information and processor

instructions containing errors that are not capable of being executed by said processing circuitry,

said programmable error correcting circuit generates corrected processor instructions in response

to said processor instructions containing errors and said error correcting information, the

corrected processor instructions being capable of being executed by said processing circuitry.

Referring to claims 3, 4, Chen discloses that the computer system forces errors that will

be of a type that the host computer system's error control logic is capable of detecting and

correcting. For example, where the computer system includes SEC DED error correcting code,

the error correction notification intentionally forces errors that are correctable using the above-

mentioned code (Col. 25, lines 29-41), which meets the limitation of said error correcting

information includes a key that enables selection of error correction specific to an error scheme

used to generate said errors, information provided in compiled computer program data in part

controls said error correction, thereby providing complementary error correction with a

combination of the error correction key and the information provided in the compiled computer

program data.

Referring to claim 13, Chen discloses that the error correction notification intentionally

forces errors that are correctable using the above-mentioned code (Col. 25, lines 29-41), which

meets the limitation of wherein instructions provided to said processor include an intentional

introduction of errors which are correctable with error correction algorithms, said correction

algorithms pre-selected according to the key.

Referring to claim 18, Chen discloses an error correction system wherein a personal

computer (Col. 6, lines 30-49) contains an error detection unit (Figure 1. The system contains

several DRAM units that store check bits that are used during the error correction process (Col.

11, lines 50-52 & Figure 1), which meets the limitation of storing error correction control

information on said chip. The error detection unit performs error detection and correction

operations on error correction code words (Col. 5, lines 3-47). If the error correction code word

contains an uncorrectable error then the instruction with the error correction code word can not

be executed, however, if the error is correctable, then the instruction is executed (Figure 7),

which meets the limitation of loading instructions of said computer program onto instruction

registers on a microprocessor chip, correcting said instructions using said error correction control

information, executing said instructions on said chip. The computer system forces errors that will

be of a type that the host computer system's error control logic is capable of detecting and

correcting, which meets the limitation of intentionally placing errors in the computer program.

For example, where the computer system includes SEC DED error correcting code, the error

correction notification intentionally forces errors that are correctable using the above-mentioned

code (Col. 25, lines 29-41.

Conclusion

7.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Benjamin E. Lanier whose telephone number is 571-272-3805.

The examiner can normally be reached on M-Th0 7:30am-5:00pm, F 7:30am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

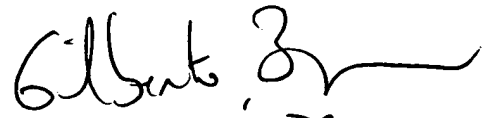Benjamin E. Lanier

GILBERTO BARRON JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100